



- +3.3V LVDS differential outputs
- Pb free and RoHS compliant assembly.
- Non-PLL circuit. 1 ps RMS phase jitter
- Pad 2 is Tri-state.



**General Specifications**

<b>Product Series</b>	<b>3HD5762</b>						
<b>Frequency Range</b>	100 MHz ~ 320 MHz. Non-PLL based.						
<b>Output Logic</b>	Differential LVDS square waves.						
<b>Frequency Stability</b>  Commercial temp. range (code "C")  Industrial temp. range (code "I")	"A": ±25 ppm over 0°C to +70°C "B": ±50 ppm over 0°C to +70°C "C": ±100 ppm over 0°C to +70°C For non-standard please specify desired frequency stability after the "C". For example "C20" is ±20 ppm over 0 to +70°C						
	"D": ±25 ppm over -40°C to +85°C "E": ±50 ppm over -40°C to +85°C "F": ±100 ppm over -40°C to +85°C For non-standard please give desired frequency stability after the "I". For example "I20" is ±20 ppm over -40 to +85°C						
	vs ±10% supply voltage change: ±3 ppm max. vs ±10% Load change: ±2 ppm max.						
<b>Supply Voltage V<sub>DD</sub></b>	+3.3 V ± 10 %						
<b>Output Voltage HIGH "1", V<sub>OH</sub></b>	1.4 V typical; 1.6 V max.						
<b>Output Voltage LOW "0", V<sub>OL</sub></b>	0.9 V min.; 1.1 V max.						
<b>Output Differential Voltage, V<sub>OD</sub></b>	247 mV min; 355 mV typical; 454 mV max. Output 1 – output 2.						
<b>Differential Output Error, dV<sub>OD</sub></b>	-50 mV min; 50 mV max.						
<b>Output Offset Voltage, V<sub>OS</sub></b>	1.125 V min; 1.2 V typical; 1.375 V max.						
<b>Offset Magnitude Error, dV<sub>OS</sub></b>	3 mV typical; 25 mV max.						
<b>Current Consumption</b>	55 mA typical; 60 mA max. for 212.50 MHz						
<b>Load</b>	50 ohms from each output.						
<b>Rise Time (Tr) and Fall Time (Tf)</b>	0.5 nano sec. typical; 0.7 nano sec. CL= 10 pF.20% ↔ 80% of the wave form.						
<b>Duty Cycle</b>	50% ± 5% max. measured at 1.25 V						
<b>Phase Jitter (RMS)</b>	1 ps max. (12 KHz to 20 MHz)						
<b>Period Jitter (RMS)</b>	<b>155.520 MHz</b>		<b>156.250 MHz</b>		<b>311.04 MHz</b>		
	typical	max.	Typical	max.	typical	max.	
	3 ps	5 ps	2 ps	3 ps	2.5 ps	4 ps	
<b>Period Jitter (Peak-to-Peak)</b>	21 ps	30 ps	18 ps	20 ps	18 ps	20 ps	
<b>Accumulated Jitter (RMS)</b>		5 ps		3 ps		4 ps	
<b>Phase Noise</b>  (offset from carrier)	<b>10 Hz Offset</b>	-72 dBc/ Hz		-75 dBc/ Hz		-60 dBc/ Hz	
	<b>100 Hz Offset</b>	-100 dBc/ Hz		-105 dBc/ Hz		-92 dBc/ Hz	
	<b>1 KHz Offset</b>	-125 dBc/ Hz		-130 dBc/ Hz		-122 dBc/ Hz	
	<b>10 KHz Offset</b>	-132 dBc/ Hz		-140 dBc/ Hz		-140 dBc/ Hz	
	<b>100 KHz Offset</b>	-142 dBc/ Hz		-145 dBc/ Hz		-142 dBc/ Hz	
	<b>1 MHz Offset</b>	-147 dBc/ Hz		-150 dBc/ Hz		-146 dBc/ Hz	
	<b>10 MHz Offset</b>	-149 dBc/ Hz		-150 dBc/ Hz		-148 dBc/ Hz	

**MERCURY** [www.mercury-crystal.com](http://www.mercury-crystal.com)

Taiwan: TEL (886)-2-2406-2779, FAX (886)-2-2496-0769, e-mail: sales-tw@mercury-crystal.com  
 U.S.A.: TEL (1)-909-466-0427, FAX (1)-909-466-0762, e-mail: [sales-us@mercury-crystal.com](mailto:sales-us@mercury-crystal.com)



<b>Start-up Time</b>		5 m sec. typical; 10 m sec. max.
<b>Aging</b>		±2 ppm / year max.
<b>Tri-state option on pad No. 2</b>	<b>No Connection</b>	LVDS and complimentary LVDS outputs.
	<b>Disable</b>	Both outputs are disabled (high impedance) when pad No. 1 is taken below 0.3 V <sub>CC</sub> referenced to ground. Oscillator is always ON. Oscillator is OFF when disabled: Available on an inquiry basis. Please contact Mercury.
	<b>Enable</b>	At disabled mode, both outputs are enabled when pad No. 1 is taken above 0.7 V <sub>CC</sub> referenced to ground.
<b>Input Static Discharge Protection</b>		2 KV max.
<b>Absolute Maximum Rating (permanent damage may be created if operate beyond limits specified)</b>		
<b>Supply Voltage V<sub>DD</sub></b>		+4.6 V D.C. max.
<b>Input Voltage V<sub>i</sub></b>		V <sub>SS</sub> -0.5V min.; V <sub>DD</sub> +0.5V max.
<b>Input Voltage V<sub>o</sub></b>		V <sub>SS</sub> -0.5V min.; V <sub>DD</sub> +0.5V max.
<b>Storage Temperature T<sub>s</sub></b>		-55°C min.; +150°C max.

<sup>(1)</sup>Inclusive of 25°C tolerance, operating temperature range, ±10% input voltage variation, load change, aging at +25°C, shock and vibration.

**Environmental Performance Specifications**

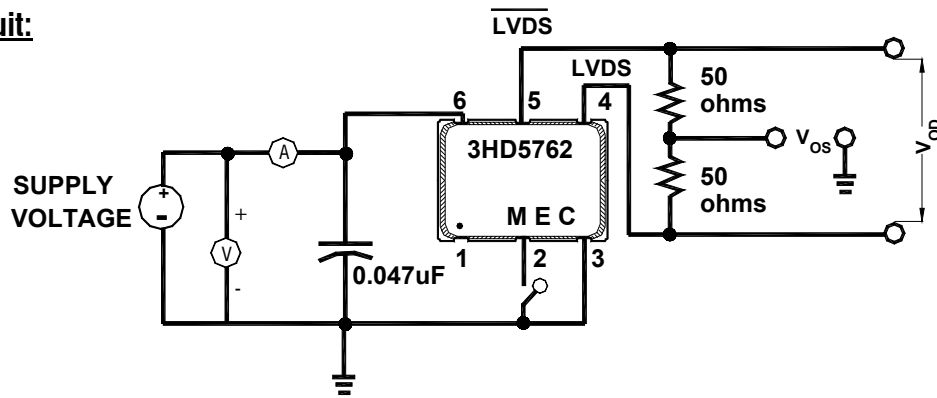
Green Requirement	RoHS Compliant and Pb (lead) free
Storage temp. range	-55 to +125°C
Humidity	85% RH, 85°C, 48 hours
Hermetic seal	Leak rate 2x10 <sup>-8</sup> ATM-cm <sup>3</sup> /sec max.
Solderability	MIL-STD-202F method 208E
Reflow	260°C for 10 sec.
Vibration	MIL-STD-202F method 204, 35G, 50 to 2000 Hz
Shock	MIL-STD-202F method 213B, test condi. E, 1000GG ½ sine wave

**Part Number Format and Example:**

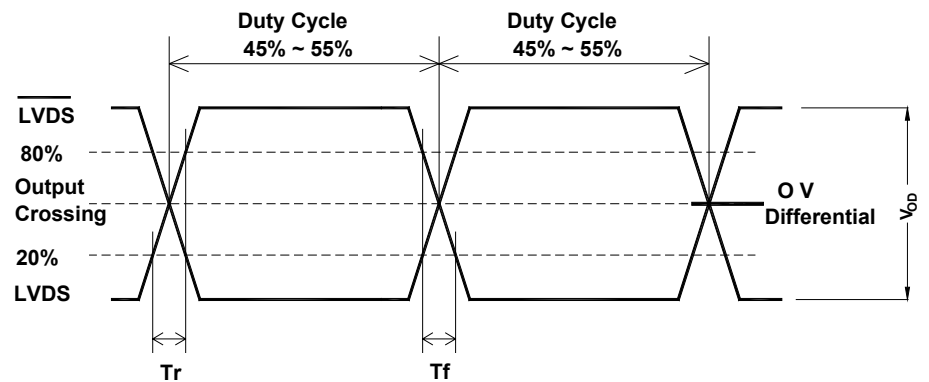
<b>Example:</b> 3HD5762-A-155.520						
<b>Explanation:</b> HD5762 LVDS clock oscillator, 5x7 mm SMD package with pad 2 as Tri-state, +3.3 V supply voltage, ±25 ppm frequency stability over 0 to +70°C, 155.520 MHz, non-PLL based						
			⌀		⌀	⌀: customer to specify
3	HD5762	—	A	—	155.520	
①	②		③		④	
①: Voltage codes: “3” for +3.3 V ②: HD5762 product series    ③: Frequency stability code: “A” ~ “F” or custom. See table above. ④: Frequency in MHz						



**HD5762 Test Circuit:**

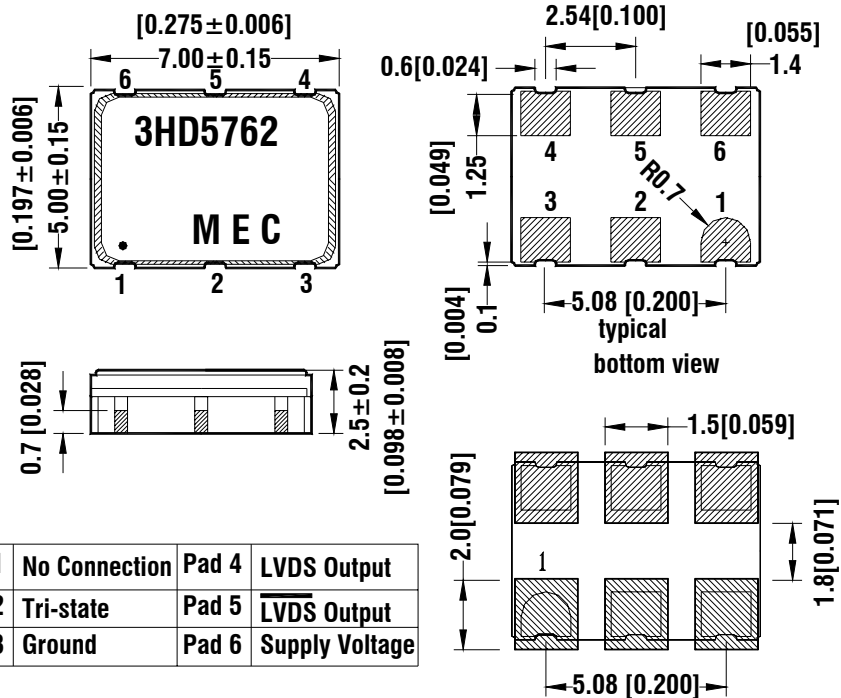


**HD5762 OUTPUT WAVEFORM:**



**HD5762 Package Dimensions and Recommended Pad Layout:**

unit mm[inches]



Pad 1	No Connection	Pad 4	LVDS Output
Pad 2	Tri-state	Pad 5	LVDS Output
Pad 3	Ground	Pad 6	Supply Voltage

Chamfered pad is pad No. 1. Count counter-clockwise when looking at top view.  
 Count clockwise when looking at bottom view.