



EM78P417/8/9N Errata document

Specification Revision History

Doc. Version	Revision Description	Date
1.0	Initial official version	2005/06/23
1.1	Added the IRC drift rate in the feature	2006/01/06
1.2	Added the EM78P418NAM SSOP 20Pins package	2006/02/22
1.3	Revised RE, RF, and IOCF0 registers contents	2006/06/01

Version 1.2 to Version 1.3

A. attached items

N.A.

B. modified items

1	Page 15~17	6.1.13 RE (WUCR: Wake-up Control Register) 6.1.14 RF (Interrupt Status Register)	Revised RE, RF registers contents
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6.1.13 RE (WUCR: Wake-up Control Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
EM78P417/8/9N	"0"	"0"	"0"	"0"	ADWE	CMPWE	ICWE	"0"
ICE418N Simulator	C3	C2	C1	C0	ADWE	CMPWE	ICWE	"0"

Bit 7 ~ Bit 4: [For EM78P417/8/9N]: Unimplemented, read as '0'

[With Simulator (C3~C0)]: IRC calibration bits in IRC oscillator mode. For ICE418N simulator, these are the IRC calibration bits in IRC oscillator mode.

C3	C2	C1	C0	Frequency (MHz)
0	0	0	0	(1-36%) x F
0	0	0	1	(1-31.5%) x F
0	0	1	0	(1-27%) x F
0	0	1	1	(1-22.5%) x F
0	1	0	0	(1-18%) x F
0	1	0	1	(1-13.5%) x F
0	1	1	0	(1-9%) x F
0	1	1	1	(1-4.5%) x F
1	1	1	1	F (default)
1	1	1	0	(1+4.5%) x F
1	1	0	1	(1+9%) x F
1	1	0	0	(1+13.5%) x F
1	0	1	1	(1+18%) x F
1	0	1	0	(1+22.5%) x F



1	0	0	1	$(1+27\%) \times F$
1	0	0	0	$(1+31.5\%) \times F$

Note: 1. Frequency values shown are theoretical and taken from an instance of a high frequency mode. Hence are shown for reference only. Definite values will depend on the actual process.
2. Similar way of calculation is also applicable to low frequency mode.

Bit 3 (ADWE): ADC wake-up enable bit
0 = Disable ADC wake-up
1 = Enable ADC wake-up

When the ADC Complete is used to wake-up EM78P417/8/9N from sleep with AD conversion running, the ADWE bit must be set to "Enable".

Bit 2 (CMPWE): Comparator wake-up enable bit
0 = Disable Comparator wake-up
1 = Enable Comparator wake-up

When the Comparator output status change is used to wake-up EM78P418/9N from sleep, the CMPWE bit must be set to "Enable".

Bit 1 (ICWE): Port 6 input change to wake-up status enable bit
0 = Disable Port 6 input change to wake-up status
1 = Enable Port 6 input change wake-up status

When the Port 6 Input Status Change is used to wake-up EM78P417/8/9N from sleep, the ICWE bit must be set to "Enable".

Bit 0: Not implemented, read as '0'

6.1.14 RF (Interrupt Status Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIF	PWM3IF	PWM2IF	PWM1IF	ADIF	EXIF	ICIF	TCIF

NOTE

- "1" means interrupt request; "0" means no interrupt occurs.
- RF can be cleared by instruction but cannot be set.
- IOCF0 is the interrupt mask register.
- Reading RF will result to "logic AND" of RF and IOCF0.

Bit 7 (CMPIF): Comparator interrupt flag. Set when a change occurs in the Comparator output. Reset by software.

Bit 6 (PWM3IF): PWM3 (Pulse Width Modulation) interrupt flag. Set when a selected period is reached. Reset by software.

<p>Bit 5 (PWM2IF): PWM2 (Pulse Width Modulation) interrupt flag. Set when a selected period is reached. Reset by software.</p> <p>Bit 4 (PWM1IF): PWM1 (Pulse Width Modulation) interrupt flag. Set when a selected period is reached. Reset by software.</p> <p>Bit 3 (ADIF): Interrupt flag for analog to digital conversion. Set when AD conversion is completed. Reset by software.</p> <p>Bit 2 (EXIF): External interrupt flag. Set by falling edge on /INT pin. Reset by software.</p> <p>Bit 1 (ICIF): Port 6 input status change interrupt flag. Set when Port 6 input changes. Reset by software.</p> <p>Bit 0 (TCIF): TCC overflow interrupt flag. Set when TCC overflows. Reset by software.</p>
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2	Page 24	6.2.11 IOCF0 (Interrupt Mask Register)	Revised IOCF0 register contents
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6.2.11 IOCF0 (Interrupt Mask Register)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMPIE	PWM3IE	PWM2IE	PWM1IE	ADIE	EXIE	ICIE	TCIE

NOTE

- IOCF0 register is both readable and writable
- Individual interrupt is enabled by setting its associated control bit in the IOCF0 to "1."
- Global interrupt is enabled by the ENI instruction and is disabled by the DISI instruction. Refer to Fig. 6-8 (Interrupt Input Circuit) under Section 6.6 (Interrupt).

Bit 7 (CMPIE): CMPIF interrupt enable bit

0 = Disable CMPIF interrupt

1 = Enable CMPIF interrupt

When the Comparator output status change is used to enter interrupt vector, the CMPIE bit must be set to "Enable".

Bit 6 (PWM3IE): PWM3IF interrupt enable bit

0 = Disable PWM3 interrupt

1 = Enable PWM3 interrupt

Bit 5 (PWM2IE): PWM2IF interrupt enable bit

0 = Disable PWM2 interrupt

1 = Enable PWM2 interrupt

Bit 4 (PWM1IE): PWM1IF interrupt enable bit

0 = Disable PWM1 interrupt

1 = Enable PWM1 interrupt

Bit 3 (ADIE): ADIF interrupt enable bit

0 = Disable ADIF interrupt

1 = Enable ADIF interrupt

When the ADC Complete is used to enter interrupt vector, the ADIE bit must be set to "Enable".

Bit 2 (EXIE): EXIF interrupt enable bit

0 = Disable EXIF interrupt

1 = Enable EXIF interrupt

Bit 1 (ICIE): ICIF interrupt enable bit

0 = Disable ICIF interrupt

1 = Enable ICIF interrupt

If Port 6 Input Status Change Interrupt is used to enter interrupt vector, the ICIE bit must be set to "Enable".

Bit 0 (TCIE): TCIF interrupt enable bit.

0 = Disable TCIF interrupt

1 = Enable TCIF interrupt

C. deleted items

N.A.