義隆電子股份有限公司
ELAN MICROELECTRONICS CORP.

HSIN-CHU: NO. 12 INNOVATION 1ST. RD
SCIENCE-BASED INDUSTRIAL PARK,
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Approved Form of Code in EM78259N

U8259N- _____(Filled in by ELAN Sales)

The Following Items Filled in by Customer

1. Customer's name: _____.
2. Name of Program File: _____.CDS.
   Checksum : _____.
3. Code Option Checksum,
   Code Option 0: _____, Code Option 1: _____, Code Option 2: _____.
4. Code Option Register (Please mark with " √ " in the adequate blank)

Code Option 0

Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Mnemonic	**–**	**–**	**–**	**TYPE**	**CLKS**	**ENWDTB**	**OSC2**	**OSC1**	**OSC0**	**HLP**	**-**	**-**	**-**
Function	High	High	High	259N	4clocks	Disable	High	High	High	High Power			
1	√	√	√	√									
Function	Low	Low	Low		2clocls	Enable	Low	Low	Low	Low Power			
0											√	√	√

Code Option 1

Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Mnemonic	**–**	**–**	**RCOUT**	**NRHL**	**NRE**	**WDTPS**	**CYES**	**C3**	**C2**	**C1**	**C0**	**RCM1**	**RCM0**
Function	High	High	High	32/fc	Enable	18ms	2 Cycles	High	High	High	High	High	High
1	√	√						√	√	√	√		
Function	Low	Low	Low	8/fc	Disable	4.5ms	1 Cycle	Low	Low	Low	Low	Low	Low
0													

Code Option 2

Bit	12	11	10	9	8	7	6	5	4	3	2	1	0
Mnemonic	**ID12**	**ID11**	**ID10**	**ID9**	**ID8**	**ID7**	**ID6**	**ID5**	**ID4**	**ID3**	**ID2**	**ID1**	**ID0**
Function	High	High	High	High	High	High	High	High	High	High	High	High	High
1													
Function	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low	Low
0													

*The range of the operating voltage: _____V.

5. Package Type: ( ) P-DIP18; ( )N-SOP18; ( )H-DIE18.
6. Intellectual Property Rights:

   The customer (hereinafter "Party A") warrants that the product/code cosigned for manufacturing by ELAN Microelectronics Corporation (hereinafter "ELAN") are self-developed or legally assigned from third parties.

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7. Delivery Schedule: Date _____, Q'TY _____ PCS

Signature Customer: _____ Date: _____Tel : _____

ELAN Sales: _____ Date: _____

ELAN FAE_____ Date: _____

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Appendix 1: The Description of the Code Option Word

EM78259N has two CODE option words and one Customer ID word that are not a part of the normal program memory.

Code Option 0	Code Option 1	Code Option 2
Bit12~Bit0	Bit12~Bit11	Bit12~Bit0

1. Code Option Register (Code Option 0)

Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
–	–	–	TYPE	CLKS	ENWDTB	OSC2	OSC1	OSC0	HLP	-	-	-

• **Bit 12 ~ 10:** Not used (reserved).
These bits are set to “1” all the time

• **Bit 9 (TYPE):** Type selection.
1 = EM78259N

• **Bit 8 (CLKS):** Instruction time period option bit
0 = two oscillator time periods
1 = four oscillator time periods (default)

• **Bit 7 (ENWDTB):** Watchdog timer enable bit
0 = Enable
1 = Disable (default)

• **Bit 6, 5 & 4 (OSC2, OSC1 & OSC0):** Oscillator Modes Selection bits

Mode	OSC2	OSC1	OSC0
ERC[1] (External RC oscillator mode); P54/OSCO acts as P54	0	0	0
ERC[1] (External RC oscillator mode); P54/OSCO acts as OSCO	0	0	1
IRC[2] (Internal RC oscillator mode); P54/OSCO acts as P54	0	1	0
IRC[2] (Internal RC oscillator mode); P54/OSCO acts as OSCO	0	1	1
LXT[3] (Low XTAL oscillator mode)	1	1	0
HXT[3] (High XTAL oscillator mode) (default)	1	1	1

[1] Under ERC mode, OSCI is used. P54 is defined by code option WORD0 Bit6 ~ Bit4.
[2] Under IRC mode, P55 is normal I/O pin. P54 is defined by code option WORD0 Bit6 ~ Bit4.
[3] Under LXT, HXT, and ERC mode; OSCI and OSCO are used.These oscillator modes cannot use normal I/O pin.

NOTE
The transient point of system frequency between HXT and LXY is around 400 KHz.

• **Bit 3 (HLP):** Power consumption selection
0 = Low power consumption, applies to working frequency at 4MHz or below 4MHz.
1 = High power consumption, applies to working frequency above 4MHz.

• **Bit 2 ~ 0:** Reserved.
The bit 2 ~ 0 set to “0” all the time.

2. Code Option Register (Code Option 1)

Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
–	–	RCOUT	NRHL	NRE	WDTPS	CYES	C3	C2	C1	C0	RCM1	RCM0

• **Bits 12 ~ 11:** Not used (reserved). These bits are set to “1” all the time

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• **Bit 10 (RCOUT):** System clock output enable bit in IRC or ERC mode
0 = OSCO pin is open drain
1 = OSCO output system clock

• **Bit 9 (NRHL):** Noise rejection high/low pulses define bit. INT pin is falling edge trigger
0 = Pulses equal to 8/fc [s] is regarded as signal.
1 = Pulses equal to 32/fc [s] is regarded as signal. (default)
NOTE
The noise rejection function is turned off under the LXT and sleep mode.

• **Bit 8 (NRE):** Noise rejection enable
0 = disable noise rejection
1 = enable noise rejection (default). However under Low XTAL oscillator (LXT) mode, the noise rejection circuit always disabled.

• **Bit 7 (WDTPS)**: WDT Time-out Period Selection bit

WDT Time	Watch-Dog Time*
1	18 ms
0	4.5 ms

*Theoretical values, for reference only

• **Bit 6 (CYES):** Instruction cycle selection bit
0 = one instruction cycle
1 = two instruction cycles (default)

• **Bits 5, 4, 3 & Bit2 (C3, C2, C1, & C0):** Calibrator of internal RC mode.
These bits must always be set to “1” only (auto calibration)

• **Bit 1 & Bit 0 (RCM1 & RCM0):** RC mode selection bits

RCM 1	RCM 0	Frequency(MHz)
1	1	4
1	0	8
0	1	1
0	0	455kHz

3. Customer ID Register (Code Option 2)

Bit 12~Bit 0
XXXXXXXXXXXXX

• **Bits 12 ~ 0:** Customer’s ID code